MULTIMEDIA UNIVERSITY

STUDENT ID NO									
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Table No.	

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2018/2019

PDS0101 – INTRODUCTION TO DIGITAL SYSTEMS

(All sections / Groups)

1 MARCH 2019
3 PM – 5 PM
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 9 pages including cover page with 5 Questions. Please attempt **ALL** questions.

2. The total marks for this paper is 50 marks.

3. Please print all your answers in this booklet.

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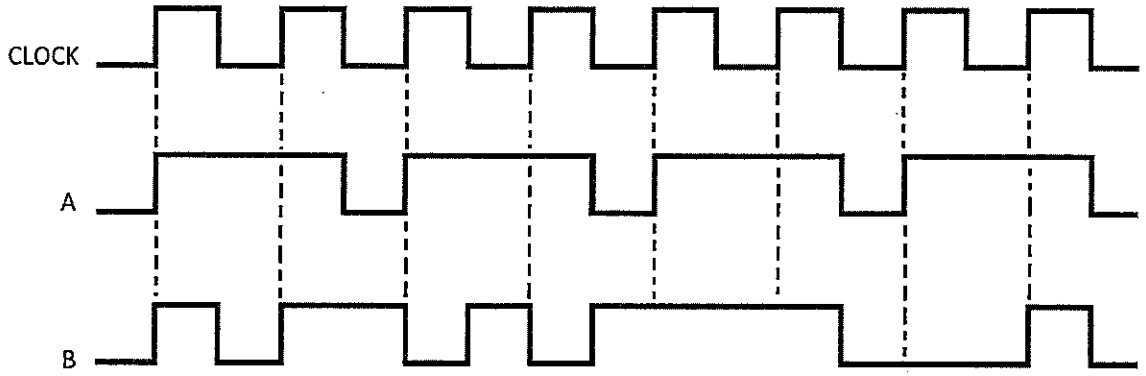
QUESTION 1



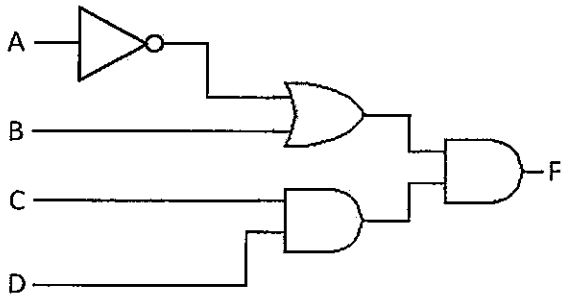
a) Referring to the above waveform image:
   i. Determine if waveform A and B are periodic or non-periodic. State your reason.
   ii. Indicate the sequence of bits for the waveforms A and B if a bit is read upon the clock's rising edge.
   iii. If the frequency of the clock is 50Hz, what is its period T?
   iv. What is the duty cycle of A? [5 Marks]

b) Perform the following operations referring to the A and B found in (a)
   i. Convert A to octal.
   ii. Convert B to hexadecimal. [2 Marks]

c) Perform the calculation of $63_{10} - 125_{10}$ using 8-bits signed 2's complement binary numbers and provide your answer in decimal. [3 Marks]

Continued .....

QUESTION 2



a) Find the Boolean expression F from the circuit given above. [1 Mark]

b) Identify the standard Sum of Product (SOP) form of the expression F found in (a). [4 Marks]

c) Identify the standard Product of Sum (POS) form for the complement of expression *F* found in (a), *i.e.* $\bar{F}$. [5 Marks]

Continued .....

QUESTION 3

a) Derive the Boolean expression of F in standard Sum of Products (SOP) format for the given truth table.

Input				Output
A	B	C	D	H
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

[2 Marks]

b) Apply K-map to minimize the Boolean expression F in SOP form and draw the simplified circuit. [4 Marks]

Continued .....

c) Simplify the following expression G by applying Boolean rules and theorems, and then draw the simplified logic circuit

$$G = \bar{A}BCD + A\bar{B}CD + ABCD$$

[4 Marks]

QUESTION 4

a) What is the difference between half-adder and full-adder? [1 Mark]

b) Construct truth table for half-adder and full-adder. [3 Marks]

Continued .....

c) Draw circuit diagram for half-adder and full-adder. [4 Marks]

d) If 1 full-adder has 8ns delay, what is the total delay time for 4-bits addition process with carry bits exist? [1 Mark]

Continued .....

e) Draw a circuit diagram for simple active-HIGH decoder that is activated with 1010 input. [1 Mark]

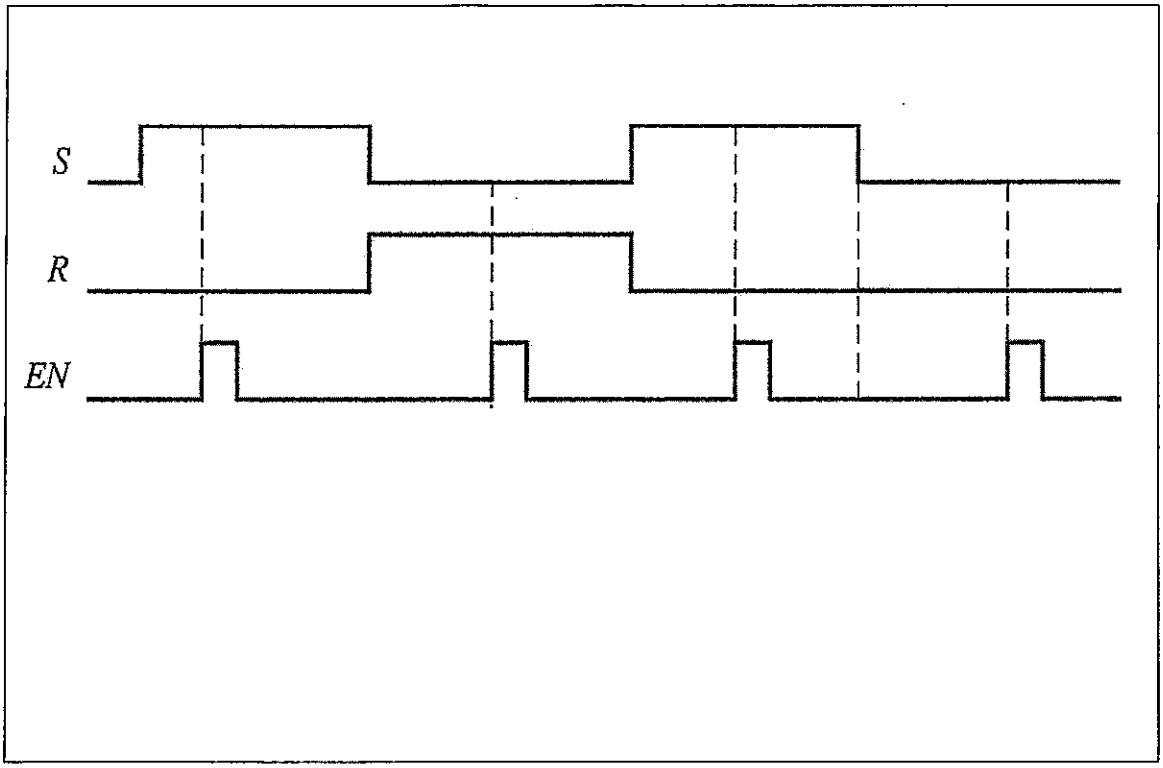
QUESTION 5

a) Draw a truth table for active-LOW S-R latch [2 Marks]

b) Draw a logic symbol for gated active-LOW S-R latch [1 Mark]

Continued .....

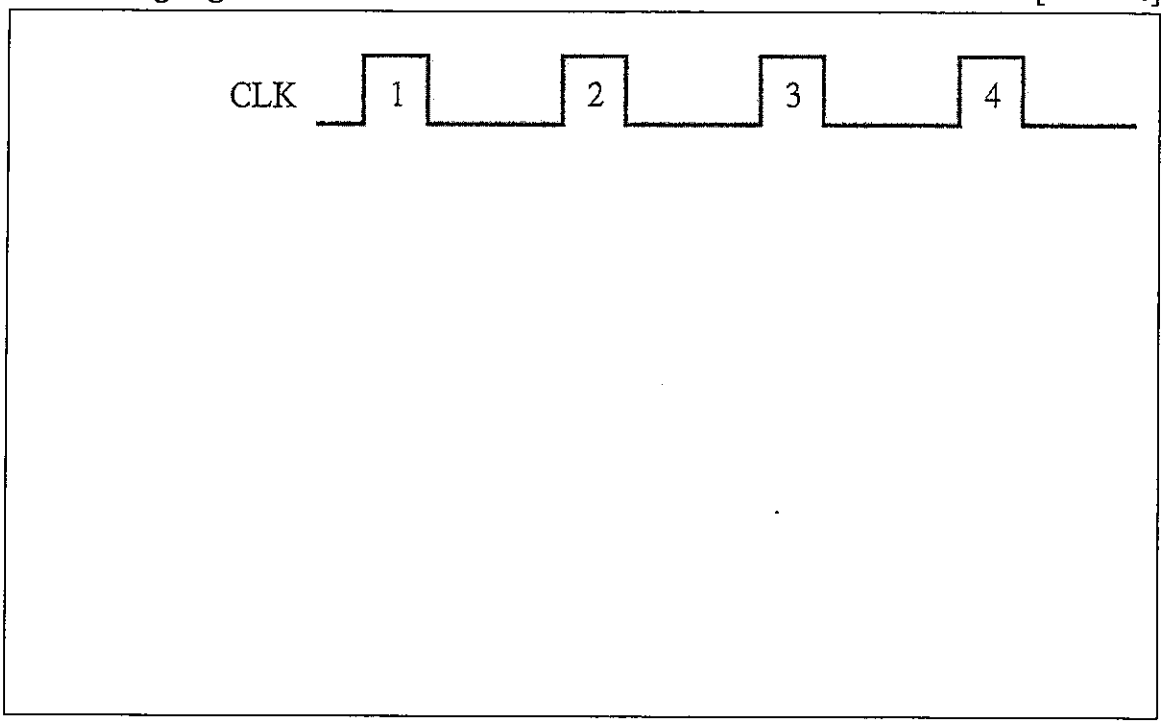
c) Given this timing diagram, draw the **Q output** for gated S-R latch. [2 Marks]



d) Draw a circuit diagram for 2-bit asynchronous counter using JK flip-flop counting up. [2 Marks]

Continued .....

e) Given 4 clock pulses for 2-bit asynchronous counter, complete the timing diagram with Q_0', Q_0, and Q_1. Assuming that this is positive going transition counter which depends on rising edge. [3 Marks]



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